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Utilizing charge reconfigurations of quantum-dot cells in building blocks to design nanoelectronic adder circuits☆

M.M. Abutaleb

Department of Electronics and Communications, Faculty of Engineering, Helwan University, Cairo, Egypt

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ABSTRACT

In the quantum-dot cellular automata (QCA) nanotechnology, the cell-based building block can be designed by utilizing the charge reconfiguration of quantum-dot cells in order to achieve the desired function with optimal implementation. In this paper, new advanced nanostructures based on quantum-dot cells are introduced to three-input XOR gate and two-to-one multiplexer, which can be considered in addition to the conventional majority voter as basic building blocks used in implementing well-optimized QCA circuits. Consequently, these blocks are used in this paper to implement new single-layer QCA full-adders and four-bit adders as motivational applications. Moreover, an innovative design approach of full-adder is proposed to avoid the presence of inputs surrounded by QCA cells and to prevent the use of crossovers when building multi-bit adders. The proposed QCA layouts are simulated and evaluated as results indicate that proposed designs are superior to the previous designs in the literature.

1. Introduction

Quantum-dot cellular automata (QCA) is a promising model of computation, which achieves excellent properties for various nanoscale computing architectures such as extremely low power dissipation and high operating speed [1]. Two embedded charged particles, electrons, can change their positions at four adjacent quantum-dots within a single QCA cell, quantum-box, resulting in two polarization states {$P = -1$ and $P = +1$} and two orientation types {45° and 90°} as shown in Fig. 1a [2]. While these charged particles cannot transfer among neighboring quantum-boxes, which means that there is no current flow in any configuration of QCA cells and that the process allows a minimum of energy to perform different functions in QCA-based circuits [2].

The QCA wire is composed of a series of cells that can be described in two different ways as illustrated in Fig. 1b: along with the same polarizations, or cross-polarization with the opposite. All QCA cells belonging to one of the four consecutive clocking zones shown in Fig. 1c execute a definite task, which in turn act as feeders for neighboring quantum-boxes assigned to the following zone [3]. QCA wires can be intersected in a single layer using two types of crossovers as shown in Fig. 2: coplanar crossing by two wires implemented using normal and rotated cells, or by two wires assigned to non-consecutive clocking zones.

The electrostatic repulsion is the expected interaction between electrons of neighboring cells to ensure the maximum separation distance. The electrostatic interaction between QCA cells is determined in various configurations using the excitation energy (kink) [4]. $E_{x,y}$ is the electrostatic energy between two electrons located in dot x and y that can be calculated

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E-mail address: mustafa_abotaleb@h-eng.helwan.edu.eg

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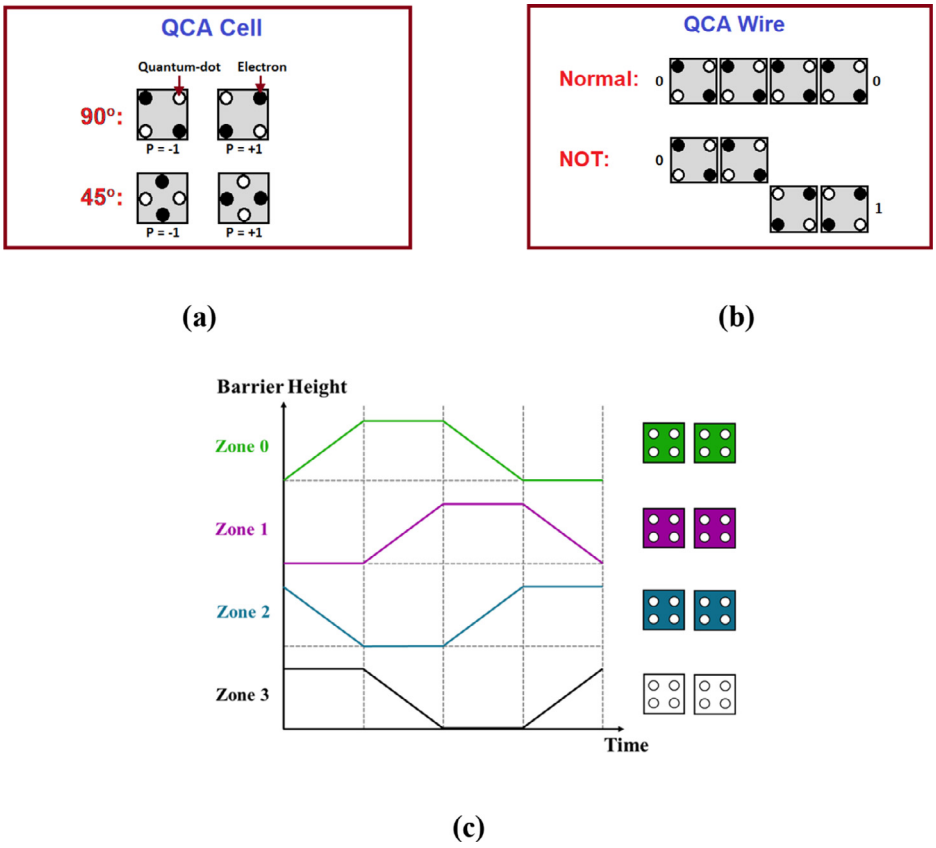


Fig. 1. Basics: (a) cell-types, (b) wire-types, (c) clock-zones.

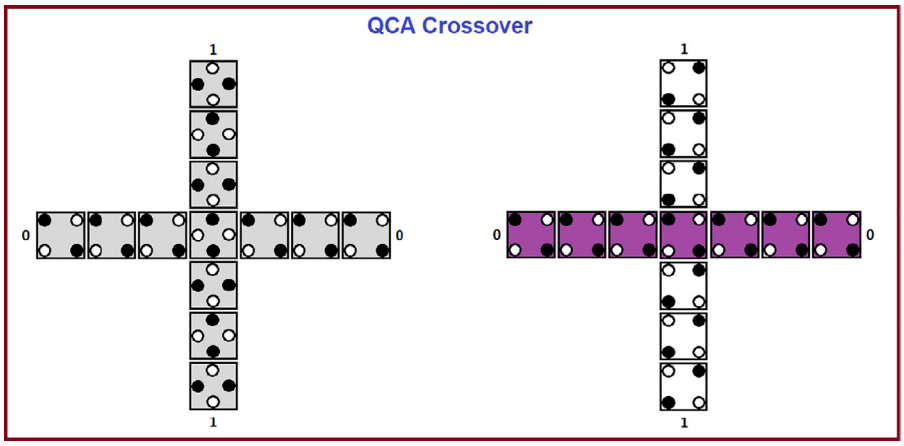


Fig. 2. QCA coplanar crossover types.

using the Eq. (1a) [4]. Where ε, d, and q are, respectively, the material system permittivity, the separation length between dot x and y, and the electron charge. The total electrostatic energy E_x^T of dot x can be computed due to N neighboring dot electrons at the effecting area by using Eq. (1b). Then the kink-energy can be calculated as the variance in total energy of two cell polarizations. In the normal QCA system, the cell has a polarization state with a lower energy for the stability. The processing of binary information within QCA configurations is based on the accumulated kink-energy principle established by electrostatic interactions between adjacent cells.

$$E_{x,y} = \frac{1}{4\pi\varepsilon}\frac{q^2}{d} \tag{1a}$$

$$E_x^T = \sum_{y=1}^{N} E_{x,y} \tag{1b}$$

From the physical design perspective, there are important issues about operating the circuits related to noise, especially when designing large circuits [5]. Long-term wires are exposed to noise and may indicate back propagation. The problem of noise coupling lies when using different orientation types and multiple layers of QCA cells in design. Therefore, the coplanar crossover using normal and rotated cells is very sensitive to noise coupling. Signals can beat the racing noise coupling across the circuit by arranging identical cells in a single layer with appropriate assignment of clock-zones. These points must be taken into consideration in order to get the correct operation and effective performance of proposed designs in QCA. Recently, many attempts have been made to implement well-organized digital gates and circuits based on QCA nanotechnology [6-10].

New design methodologies must be introduced to the QCA to take advantage of its unique characteristics and demonstrate the expected benefits from technological and architectural perspectives. However, many research proposals have been presented to build electronic circuits, most of which rely on a so-called gate-based design style. This methodology is based on the use of a majority gate, which when used in complex circuits leads to an increase in size, time delay and energy consumption. Therefore, this paper presents a proposal for a new design methodology that relies on cell-based building blocks. This idea is based on the possibility of achieving the desired function using the charge reconfiguration of quantum-dot cells within the suitable QCA nanostructures. Therefore, the difficulty encountered in this research is to choose the basic building blocks while achieving the optimal implementation of each block with the consideration that the QCA layout must be realized based on the explicit interaction of cells to yield the wanted function.

Through extensive study and comprehensive research, any digital circuit can be implemented using one or more blocks of majority voters, XOR gates and multiplexers. The XOR gate is a single-output block that switches to Logic 1 when the number of active inputs is odd, while the multiplexer is a block that selects one of multiple inputs based on controls and transfers it to its output. In this paper, new advanced nanostructures based on quantum-dot cell are introduced to three-input XOR gate and two-to-one multiplexer. These cell-based building blocks can be broadly applied to QCA-based circuit designs to achieve improvements. As motivational applications in this paper, the QCA adder circuits are designed based on proposed blocks. The principal contributions of this paper can be outlined as follows.

1. The cell-based block of three-input XOR gate is defined in QCA.
2. The cell-based block of two-to-one multiplexer is defined in QCA.
3. The novel full-adder circuit is implemented based on QCA cell-based blocks.
4. The optimal full-adder layout is compared to others and improvements are identified.
5. New ripple carry adders are also introduced and applied in QCA.
6. Proposed ripple carry adders are compared to others and improvements are identified.

This paper is organized as follows. The QCA cell-based implementation procedure for building blocks is presented in Section 2. The optimization of QCA-based full-adder circuit is explained in Section 3. QCA design approaches along with the utilization of building blocks in the design of the ripple carry adders are explored in Section 4. Finally, Section 5 provides conclusive remarks that succinctly summarizes the paper.

2. Cell-based building blocks

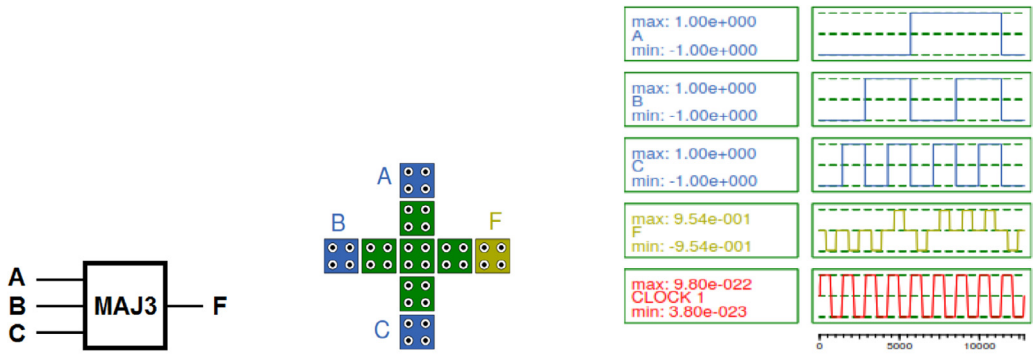
There are a number of key elements that can be used as basic building blocks to build more complex circuits in QCA. In the implementation of QCA circuits, the greatest important building blocks are majority voter, XOR gate, and multiplexer that are utilized to implement the nanoscale circuits with unique features including very low power consumption and high operating speed. In this section, QCA building blocks are performed using a cell-based approach in order to achieve the desired function by utilizing the charge reconfiguration of quantum-dot cells.

2.1. Conventional majority voter

Three-input majority (MAJ3) voter is a considered as the conventional building block in most of QCA-based circuit designs. The graphic symbol of MAJ3 voter with three inputs and one output is outlined in Fig. 3a. Its logic operation can be represented by Eq. 2. This gate can be configured as AND/OR function by assigning a feed signal to logic 0/1. Two-input AND and OR gates can be configured using the MAJ3 voter by assigning one of voter inputs as logic 0 and 1, respectively, and the other two inputs become the gate terminals.

$$F = \mathrm{MAJ3(A,\ B,\ C)} = \mathrm{AB + AC + BC} \tag{2a}$$

$$F = \mathrm{MAJ3(A,\ B,\ 0)} = \mathrm{AND2(A, B)} = \mathrm{AB} \tag{2b}$$



(a) (b) (c)

Fig. 3. MAJ3 voter: (a) graphic diagram, (b) implementation, (c) simulation result.

Table 1
Truth table of MAJ3 voter.

Input			Output
A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

$$F = \text{MAJ3}(A,\ B,\ 1) = \text{OR2}(A, B) = A + B \tag{2c}$$

The QCA configuration of this building block is appeared in Fig. 3b with feed signals {A,B,C} and output signal {F}. It comprises of 9 cells containing latency of 0.25 QCA timing cycle in an occupied area of 0.009 μm^2. It very well may be seen from Fig. 3b that the design of majority block is formed by configuring quantum-boxes in such way to vote majority inputs into the output. Table 1 shows the main task of the majority block.

Two engines {"Bistable approximation", "Coherence vector"} are used for testing QCA designs in a well-known QCA layout and simulation tool called "QCADesigner tool" [11]. A time-independent simulation is used in "Bistable approximation" engine with the law of least electrostatic energy for evaluated cell polarization, thus increasing the simulation speed in this engine. Another engine uses a time-dependent method for a cell state due to the interaction of cells [4,11]. A simulator tool that considers the physical aspects of QCA cells can greatly help in studying the propagation of signals compared to noise.

All QCA layouts in this paper are tested under each of the simulation engines in the "QCADesigner version 2.0.3″ with 5 nm for a dot diameter, 18 nm × 18 nm for a cell size, 65 nm for a radius of effect, 2 nm for a separating space between cells, and engine-based values for other parameters. The input and result signals of MAJ3 layout is provided in Fig. 3c based on the execution of QCA simulation.

2.2. Proposed exclusive-or gate

Exclusive-OR (XOR) gate is the essential building block for many circuit designs such as parity generators, data checkers, comparators, code converters, etc. The graphic symbol of three-input XOR (XOR3) gate with three inputs and one output is drawn in Fig. 4a. Its logic operation can be represented by Eq. 3. This block can be configured as XOR2/XNOR2 function by setting one of its feeders to logic 0/1.

$$\text{F} = \text{XOR3}(\text{A}, \text{B}, \text{C}) = \text{A} \oplus \text{B} \oplus \text{C} \tag{3a}$$

$$\text{F} = \text{XOR3}(\text{A},\ \text{B},\ 0) = \text{XOR2}(\text{A}, \text{B}) = \text{A} \oplus \text{B} \tag{3b}$$

$$\text{F} = \text{XOR3}(\text{A},\ \text{B},\ 1) = \text{XNOR2}(\text{A}, \text{B}) = \text{A} \odot \text{B} \tag{3c}$$

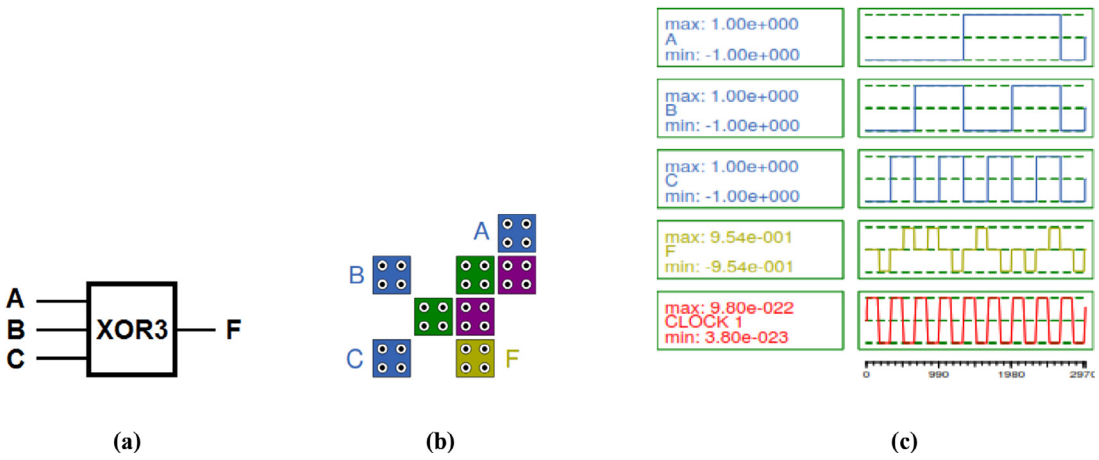


Fig. 4. XOR3 gate: (a) graphic diagram, (b) implementation, (c) simulation result.

Table 2
Truth table of XOR3 block.

Input			Output
A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

The configuration of cell-based XOR3 block is presented in Fig. 4b that has feed signals {A,B, and C} and output signal {F}. It comprises of 8 QCA cells containing latency of 0.5 timing cycle in an occupied area of 0.006 μm^2. It is possible to see clearly from Fig. 4b that the XOR3 template is formed by configuring quantum-boxes from side to side and by taking advantage of the added nature of Coulomb forces to apply the required gate. It merits making reference to that the designed component is actualized in one layer without utilizing any turned cell. Furthermore, it is implemented without using any majority voter. Thus, removing the majority of voters in this block results in planning with fewer space and lower energy consumption.

Table 2 shows the main task of the XOR3 block. The input and result signals of XOR3 layout is delivered in Fig. 4c based on the execution of QCA simulation. As is evident, the output {F} is evaluated by setting inputs A, B and C to specific values; when the total number of ones in the input vectors {ABC} is odd, then the generated output bit is 1 and otherwise, the generated output bit is 0. The output signal is noise-free according to the figure. This outcome is verified by the expected yield F in Table 2 to ensure that the designed XOR3 block is performing its function precisely.

2.3. Proposed multiplexer

A multiplexer is a significant building block in many digital applications such as data selectors, configurable logic blocks, communication systems and so on. The graphic symbol of 2-to-1 multiplexer (MUX2) is displayed in Fig. 5a. This building block has three sources {I0,I1,SEL} and creates a yield {F}. It is a two-signal choices circuit where it transfers one of inputs into the output according to SEL value as described in Eq. 4.

$$F = \ MUX2(I0,\ I1,\ SEL) = \overline{SEL}\ .I0 + SEL\ .I1 \tag{4a}$$

$$F = \ MUX2(I0,\ I1,\ 0) = I0 \tag{4b}$$

$$F = \ MUX2(I0,\ I1,\ 1) = I1 \tag{4c}$$

The corresponding design is demonstrated in Fig. 5b. It comprises of 12 QCA cells containing latency of 0.25 QCA timing cycle in an occupied area of 0.014 μm^2. It is possible to see clearly from Fig. 4b that the MUX2 template is formed by configuring quantum-boxes from side to side and by taking advantage of the added nature of Coulomb forces to apply the

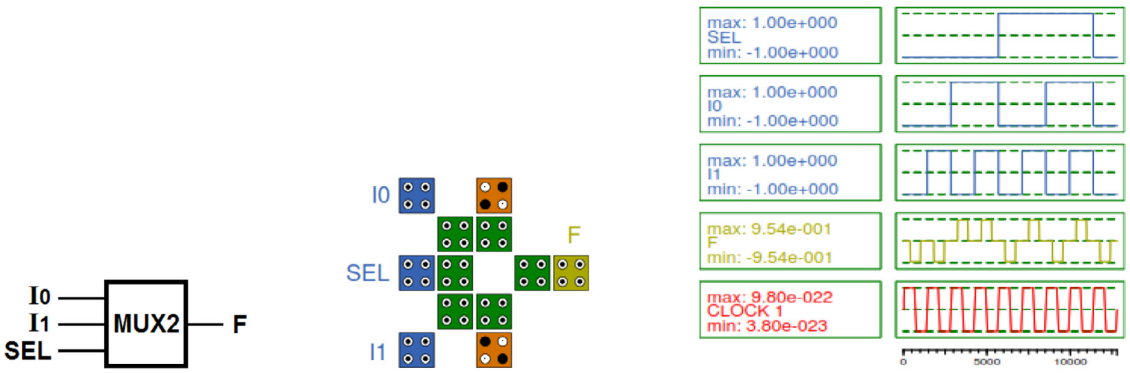


Fig. 5. MUX2: (a) graphic diagram, (b) implementation, (c) simulation result.

Table 3
Truth table of MUX2.

Input			Output
SEL	I0	I1	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Table 4
Operation table of FA circuit.

Input			Output	
A	B	C	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

required operation in a clock zone. It merits making reference to that the designed block is actualized in one layer without utilizing any turned cell. Furthermore, it is implemented without using any majority voter.

Table 3 shows the main task of the MUX2 block. The input and result signals of XOR3 layout is delivered in Fig. 5c based on the execution of QCA simulation. As is evident, the output {F} is evaluated by setting the selector input {SEL} to a specific value; $F = I0$ at $SEL = 0$ whereas, $F = I1$ at $SEL = 1$. The output signal is noise-free according to the figure. This outcome is verified by the expected yield F in Table 3 to ensure that the designed MUX2 block is performing its function perfectly.

3. Towards optimal qca full-adder circuit

In this section, a novel and efficient QCA layout is proposed for the one-bit adder circuit called the full-adder (FA). This adder is the core arithmetic module used in the implementation of multi-bit QCA adders. The FA circuit has three input bits labelled as A, B, and C (carry-in). It carries out the addition of them and produces two output bits known as S (sum) and Co (carry-out). The logical functions for sum and carry-out of full-adder are formulated using Eq. 5. The truth table of FA circuit is presented in Table 4.

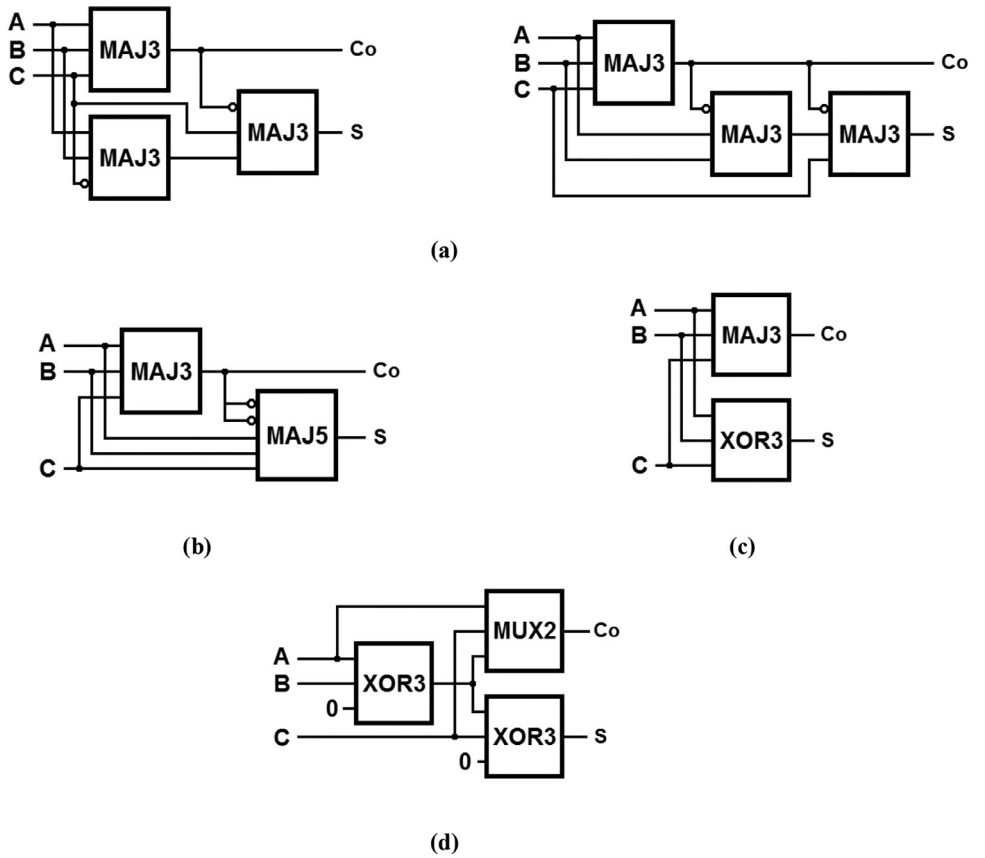


Fig. 6. Full-adder design in QCA: (a) MAJ3 based approach, (b) MAJ5-MAJ3 based approach, (c) XOR3-MAJ3 based approach, (d) proposed XOR3-MUX2 based approach.

$$S = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC \tag{5a}$$

$$\mathrm{Co} = AB + BC + AC \tag{5b}$$

3.1. Related works

Several different QCA full-adder circuits have been exhibited in the literature. In general, three design approaches have been used in implementing the sum and carry-out functions of QCA full-adder: MAJ3 based design approach, MAJ5-MAJ3 based design approach, and XOR3-MAJ3 based design approach.

QCA full-adder circuits have initially been implemented using three-input majority voters [12-16]. In this design approach, the carry-out expression is represented as shown in Eq. (6) and the sum expression can be characterized using Eq. (7a) or Eq. (7b). The block diagrams of MAJ3 based full-adder circuit are shown in Fig. 6a. As it is shown in Fig. 6a, the FA design includes three MAJ3 gates. The carry-out signal is evaluated at first and then uses its inversion signal to generate the sum signal.

$$\mathrm{Co} = \mathrm{MAJ3}(A,\ B,\ C) \tag{6}$$

$$S = \mathrm{MAJ3}\left(\mathrm{MAJ3}\left(A,\ B,\ \bar{C}\right), \overline{\mathrm{MAJ3}(A,\ B,\ C)},\ C\right) \tag{7a}$$

$$S = \mathrm{MAJ3}\left(\mathrm{MAJ3}\left(\overline{\mathrm{MAJ3}(A,\ B,\ C)},\ A,\ B\right),\ \overline{\mathrm{MAJ3}(A,\ B,\ C)},\ C\right) \tag{7b}$$

To reduce the hardware complexity, another design approach has been presented for designing full-adder circuit in QCA by using a five-input majority (MAJ5) voter [17-22]. In this approach, the carry-out and sum functions are expressed based on three- and five-input majority voters as shown in Eqs. (6) and 8, respectively. The block diagram of MAJ5-MAJ3 based FA

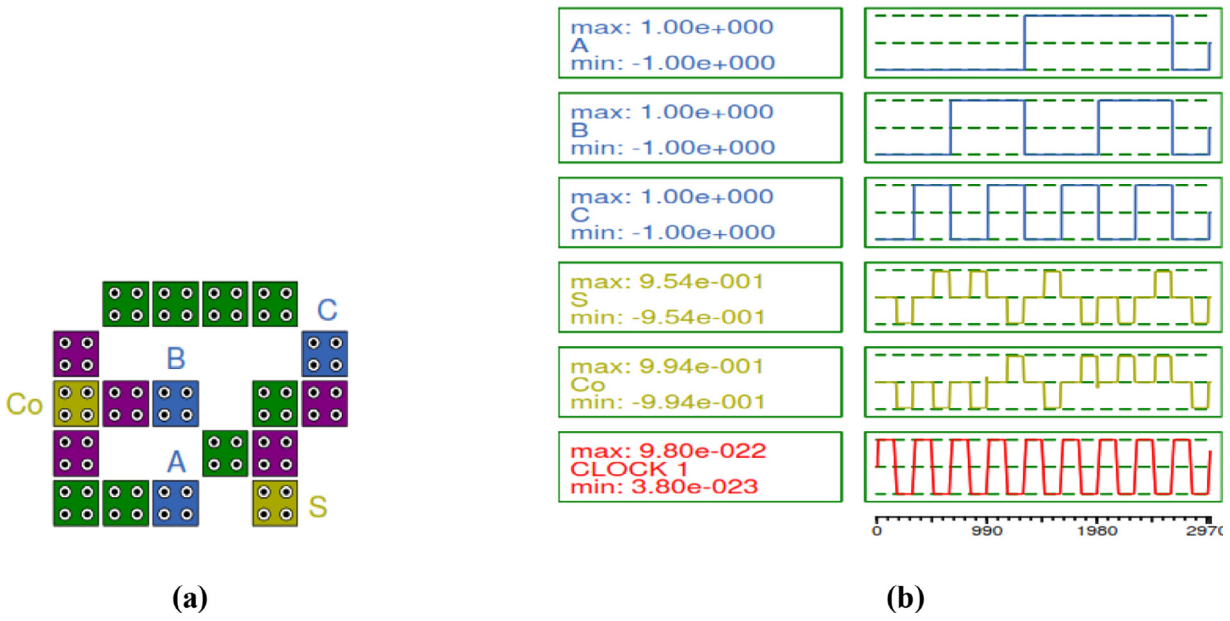


Fig. 7. Proposed FA1 circuit: (a) implementation, (b) simulation signals.

circuit is displayed in Fig. 6b. As shown in Fig. 6b, the full-adder design includes a single MAJ3 gate in the first circuit level to produce the carry-out signal and a single MAJ5 gate in the second level to produce the sum signal.

$$S = \mathrm{MAJ5}\left(\overline{\mathrm{MAJ3}(A, B, C)},\ A, \overline{\mathrm{MAJ3}(A, B, C)}, B, C\right) \tag{8}$$

Recently, the QCA-based structure has been proposed for the XOR-based FA circuit to generate a sum signal [23-25]. In this design, the carry-out and sum expressions are represented based on three-input majority voter and three-input XOR function as shown in Eqs. (6) and 9, respectively. The schematic diagram of XOR3-MAJ3 based FA circuit is presented in Fig. 6c. As it is shown in Fig. 6c, the carry-out signal is generated as the output of MAJ3 gate and the sum signal is generated as the output of XOR3 gate.

$$S = \mathrm{XOR3}(A,\ B,\ C) \tag{9}$$

3.2. Optimal design of full-adder

The optimal full-adder (FA1) circuit is proposed here in QCA using the XOR3-MAJ3 based design approach mentioned previously. The corresponding QCA layout is presented in Fig. 7a. As shown in this layout, it is designed by using two cell-based building blocks discussed in Section 2, one of them is conventional MAJ3 voter and the other is proposed XOR3 gate. The proposed layout (Fig. 7a) comprises of 18 QCA cells containing latency of 0.5 QCA timing cycle in an occupied area of 0.01 μm^2. The input and result signals of FA1 layout is delivered in Fig. 7b based on the execution of QCA simulation. As is evident, the sum {S} and carry-out {Co} outputs are evaluated according to all possible values of inputs {A, B and C}. This outcome is verified by the expected yields {S and Co} in Table 4 to ensure that the designed FA1 design is performing its function precisely.

A detailed comparison of the designed QCA FA1 circuit with recent single- and multi- layer designs reported in [14,16,20-25] is shown in Table 5. QCA structures are estimated using greatest usually acknowledged metrics including number of cells, size, and propagation delay. Here, the number of configured QCA cells specifies the circuit complexity of FA layouts. Besides, the synthesis cost of QCA layouts can be estimated using the cost function given in Eq. (10) [10,20,21]. The total occupied area in terms of μm^2 is recorded along with the latency in terms of QCA clock cycles ($\times\ 10^{-12}$ s) in this formula for rating the result in a direction of smaller and faster implemented circuit. The FA circuits are also evaluated using the QCA cost equation and corresponding results are recorded in Table 5. It is certainly that the proposed single-layer layout of full-adder FA1 has a significant progress in all aspects over the layouts recently presented in [14,16,20-25].

The full progress of designed FA1 circuit in excess of single-layer adders recorded in Table 5 is represented in Fig. 8. As shown, the FA1 layout optimizes the QCA circuit complexity (cell count) by 38% compared to the best single-layer FA circuit reported in [25]. In addition, it improves the QCA synthesis cost by 50% over the best single-layer FA circuit reported in [25]. The goal of proposing the optimal design is achieved. Therefore, the proposed FA1 module provides several basic benefits in building complex arithmetic systems in QCA, for example, one layer usage, small size, and low complexity.

$$\mathrm{Cost} = \mathrm{Area}\ \mathrm{x}\ \mathrm{Latency}^2 \tag{10}$$

Table 5
Structural comparison of QCA FA circuits.

Design approach	FA circuit	Cell count (# cells)	Area ($\times$ μm^2)	Latency ($\times$ 10^{-12} s)	QCA cost	Layer count (# layers)
MAJ3 based approach	[14]	59	0.04	1	0.040	1
	[16]	82	0.07	1	0.070	3
MAJ5-MAJ3 based approach	[20]	63	0.05	0.75	0.028	1
	[21]	45	0.04	0.5	0.010	1
	[22]	22	0.01	0.75	0.006	3
XOR3-MAJ3 based approach	[23]	41	0.04	0.5	0.010	1
	[24]	38	0.03	0.5	0.008	1
	[25]	29	0.02	0.5	0.005	1
	Proposed FA1	18	0.01	0.5	0.003	1
Proposed XOR3-MUX2 based approach	Proposed FA2	38	0.03	0.75	0.017	1

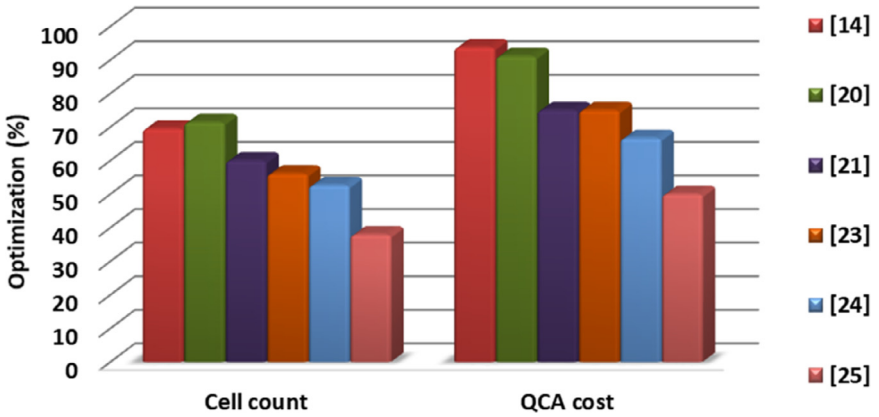


Fig. 8. Improvements of proposed FA1 over others.

4. QCA ripple carry adders

The QCA ripple carry adder (RCA) with the length of four bits is introduced in this section to demonstrate the productivity of proposed full-adder module in high-level arithmetic architectures. The 4-bit RCA is realized using four FA modules cascaded in parallel so that the terminal Co of embedded FA is linked to the terminal C of following FA.

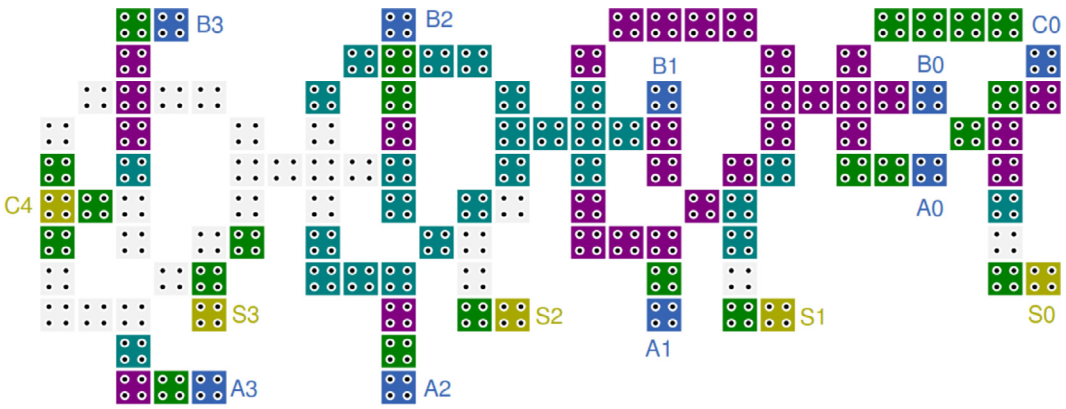
4.1. Design of RCA with coplanar crossovers

The QCA layout of proposed 4-bit RCA (RCA1) architecture based on the FA1 circuit is displayed in Fig. 9a. This layout contains 117 QCA-cells with a propagation delay of 1.25 timing cycle and an occupied area of 0.12 μm^2. It can be seen from Fig. 9a that data inputs are described as first input A(3:0), second input B(3:0), and carry-in bit C0. Whereas data outputs are labelled as sum bits S {S3,S2,S1,S0} and carry-out bit C4. Moreover, the coplanar wire crossing is performed logically for inputs B2 and B3 based on different clock zones. The proposed RCA1 uses a robust coplanar crossover to avoid noise coupling, which is an appropriate design for designing larger computational circuits.

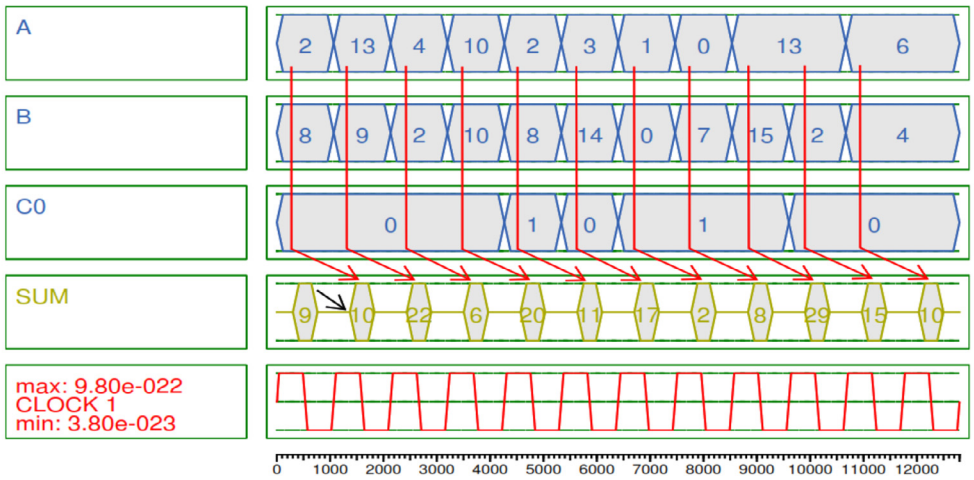
The simulation result of RCA1 is illustrated in Fig. 9b using bus representation and decimal format. This adder is tested with a specific set of input vectors. As apparent, it performs the addition of two binary numbers A(3:0) and B(3:0) with the previous carry value C0. The first valid result SUM(4:0) appears after a delay of 1.25 QCA clock cycle as shown by the black arrow. Additionally, C4 is appended in front of sum bits to show the appropriate result values by using red arrows for each applied input data. Outputs indicate that the proposed RCA1 works exactly.

4.2. Design of RCA without crossovers

Although the proposed FA1 design is characterized by its minimum size and is also the fastest, the presence of one of the inputs surrounded by cells leads to the use of coplanar crossover when building multi-bit adders. This issue exists in



(a)



(b)

Fig. 9. Proposed RCA1 circuit: (a) QCA layout, (b) simulation result.

previous designs, some of them use the coplanar crossover and others uses multilayers. So, a new approach is proposed here for designing the full-adder in order to satisfy the existence of all input and output cells without being surrounded by design cells.

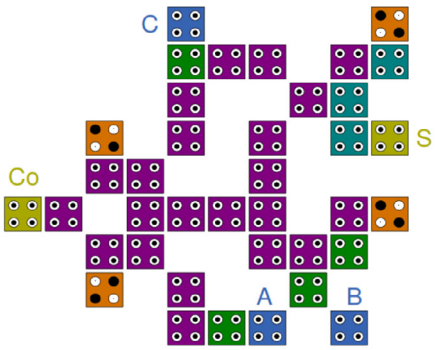
The proposed design approach uses XOR3 and MUX2 components to produce the desired sum and carry-out outputs. In the XOR3-MAJ3 based design approach, the sum and carry-out functions are expressed by Eq. 11. The schematic diagram of XOR3-MUX2 based full-adder circuit is shown in Fig. 6d. In this design approach, the SEL signal is generated at first and then uses it to produce the sum and carry-out signals.

$$\mathrm{SEL} = \mathrm{XOR3}(\mathrm{A},\ \mathrm{B},\ 0) \tag{11a}$$

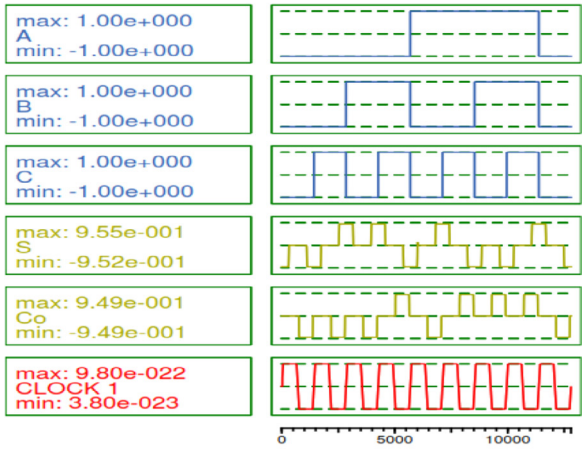
$$S = \mathrm{XOR3}(\mathrm{SEL},\ \mathrm{C},\ 0) \tag{11b}$$

$$\mathrm{Co} = \mathrm{MUX2}(\mathrm{A},\ \mathrm{C},\ \mathrm{SEL}) \tag{11c}$$

The QCA circuit of full-adder (FA2) based on this new approach is presented in Fig. 10a. As shown in this layout, it is designed by using two cell-based building blocks proposed in Section 2, one of them is MUX2 and the other is XOR3 gate. The proposed layout (Fig. 10a) contains only of 38 cells with a propagation delay of 0.75 timing cycle and an occupied area of 0.03 μm^2. It is clear that the FA2 circuit, designed in one layer with QCA structure metrics in Table 5, is close to the previous full-adders and moreover it has a unique capability as it can be extended without the use of any wire-crossing technology. It has a directed forward structure so that the input and output cells are not surrounded by other QCA



(a)



(b)

Fig. 10. Proposed FA2 circuit: (a) QCA layout, (b) simulation result.

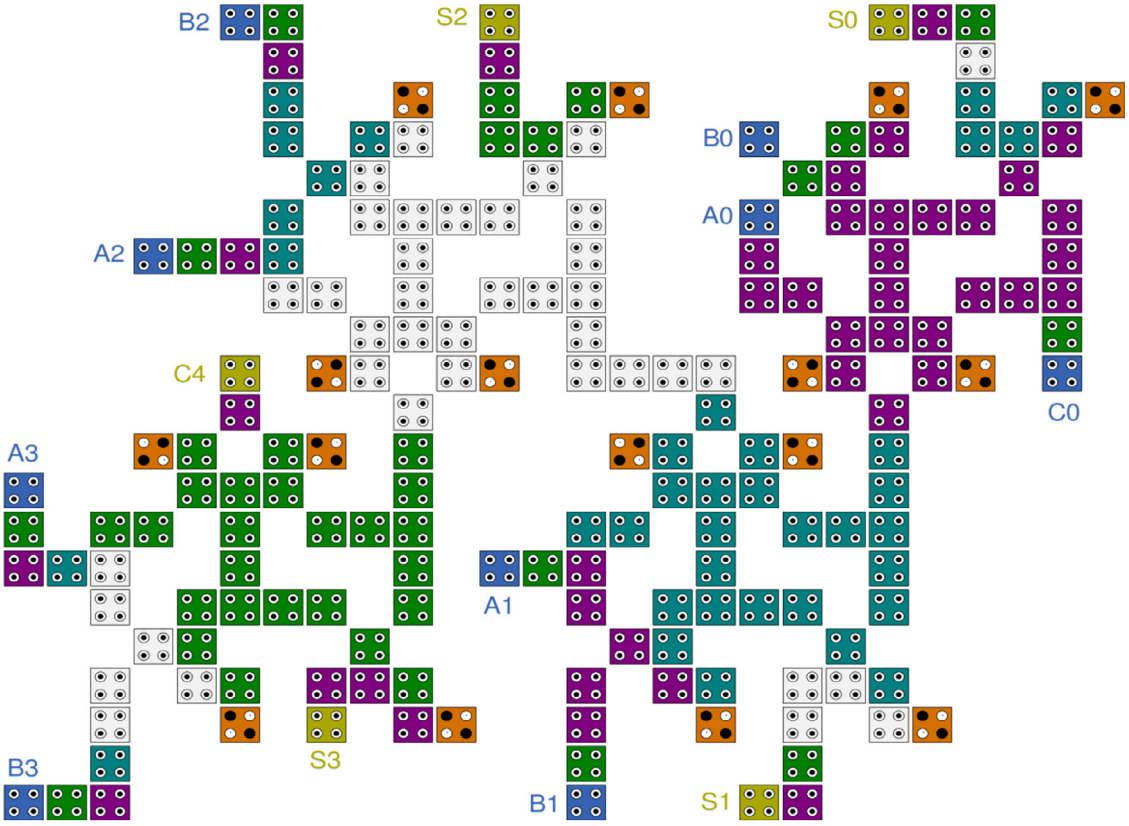
cells, facilitating high-level dense QCA arithmetic implementations. The result of simulation is depicted in Fig. 10b for the designed FA2 circuit. As is shown, output bits (S and Co) are assigned based on all possible values of input bits (A, B and C). This outcome is checked with the recorded outputs in Table 4 to ensure that the proposed FA2 design is performing its function perfectly.

The proposed 4-bit RCA (RCA2) architecture is constructed based on the FA2 circuit. The corresponding single-layer design is presented in Fig. 11a. It contains 186 QCA-cells in one layer with a propagation of 1.5 timing cycle and an occupied area of 0.22 μm^2. It is apparent that this adder is designed without using any turned cell or crossing wire. The simulation result of RCA2 layout is depicted in Fig. 11b. This adder is tested with the same set of input vectors used in testing RCA1 layout. As shown in this result, outputs indicate that the proposed RCA2 structure works correctly.

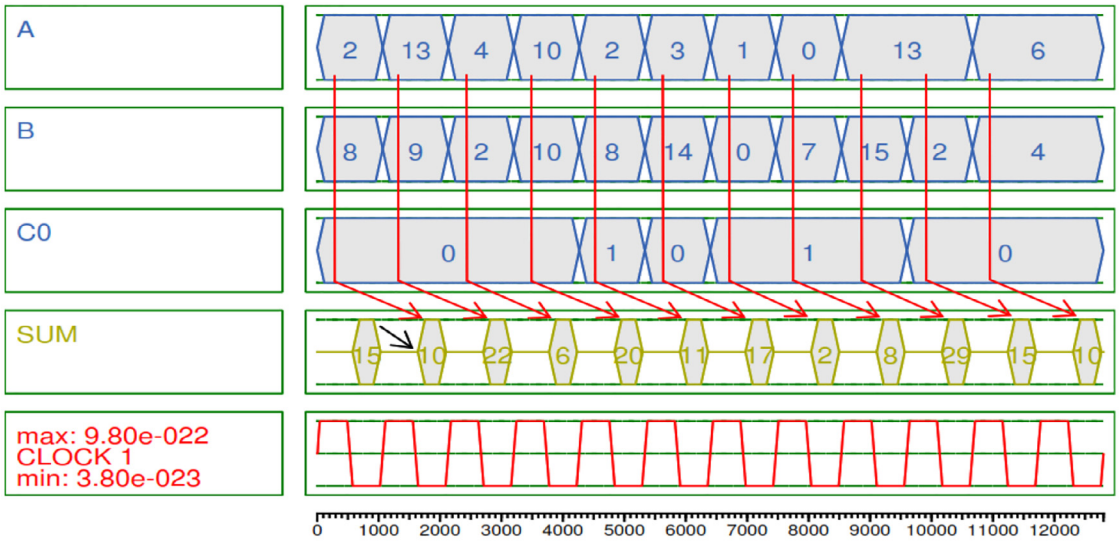
4.3. Structural analysis

To evaluate proposed FA-based arithmetic circuits, comparison results between 4-bit RCA architectures designed in this work and recently reported works are summarized in Table 6. Evidently, proposed adders have substantial superiority over RCA architectures reported recently in [14,20,21,25].

The overall improvements of proposed QCA RCA layouts over previous single-layer structures listed in Table 6 are depicted in bar-graph forms as shown in Fig. 12. As it is apparent from this figure, the proposed single-layer QCA layout of RCA1 achieves 55% and 71% improvements in cell count and overall cost, respectively, as compared to the best structure reported in [14]. In comparison with this best structure, the advancements achieved for the designed RCA2 circuit are 23% and 29% enhancements in whole QCA cost and number of quantum-dot cells, respectively, without utilizing any wire-crossing type. Overall, the results specify superb enhancements in the proposed FA-based RCA structures over newly proposed QCA-based structures.



(a)



(b)

Fig. 11. Proposed RCA2 circuit: (a) QCA layout, (b) simulation result.

Table 6
Structural comparison of QCA 4-bit RCA architectures.

4-bit RCA	Cell count (# cells)	Area ($\times$ μm^2)	Latency ($\times$ 10^{-12} s)	QCA cost	Crossover type
[14]	262	0.21	1.75	0.64	Coplanar
[20]	295	0.3	1.5	0.68	Coplanar
[21]	314	0.32	1.5	0.72	Multilayer
[25]	269	0.37	3.5	4.53	Coplanar
Proposed RCA1	117	0.12	1.25	0.19	Coplanar
Proposed RCA2	186	0.22	1.5	0.50	Not exist

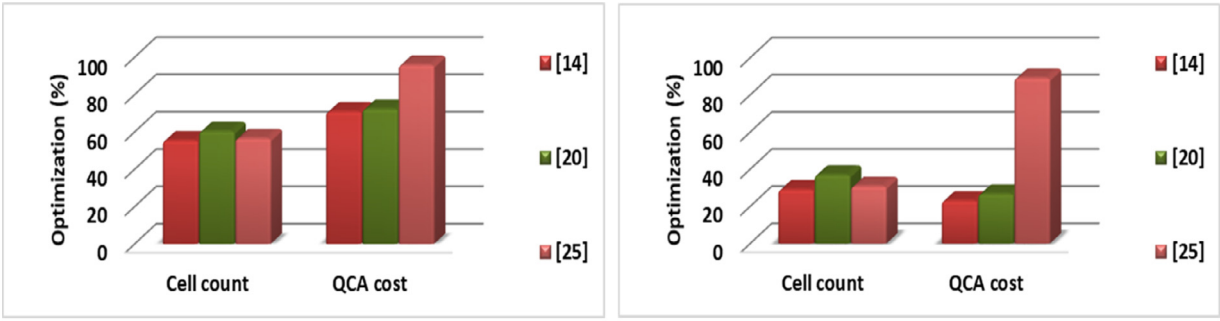


Fig. 12. Improvements of proposed 4-bit RCA over others: (a) RCA1, (b) RCA2.

5. Conclusions

In this paper, novel nanoscale structures for three-input XOR gate and two-to-one multiplexer have been introduced in QCA in order to achieve the appropriate functions based on charge reconfigurations of integrated cells. Using these cell-based building blocks, two single-layer QCA full-adders have been implemented. The first proposed full-adder (FA1) has been implemented based on the XOR3-MAJ3 approach with 38% improvements in circuit complexity and 50% in synthesis cost compared to the best single-layer QCA full-adder reported in the literature. A new XOR3-MUX2 based design approach has been introduced in this work for designing the second proposed full-adder (FA2) where all input and output cells located outside the design. Furthermore, two QCA architectures have been introduced for a four-bit ripple carry adder (RCA) as an application for high-level computational circuits. All proposed single-layer QCA layouts have been simulated and evaluated based on most widely accepted metrics and functions. The results have yielded significant improvements compared to previous corresponding architectures in the literature. The first proposed ripple carry adder (RCA1) has been performed based on the FA1 module with 55% improvements in circuit complexity and 71% in synthesis cost compared to the previous best work for the single-layer QCA RCA design. The second proposed ripple carry adder (RCA2) has been performed based on the FA2 module with 29% improvements in circuit complexity and 23% in synthesis cost compared to the best single-layer QCA adder mentioned in the literature in addition to a unique feature of this design which is not to use any type of crossovers. It very well may be reasoned that the utilization of proposed blocks in high-level designs leads to considerable optimizations in hardware complexity aspects.

Declaration of Competing Interest

None

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M.M. Abutaleb was born in Cairo, Egypt, in 1979. He received the B.*Sc*., M.*Sc*. and Ph.D. degrees in Electronics and Communications Engineering from Helwan University, Cairo, Egypt, in 2001, 2005 and 2010, respectively. Currently, he is an Associate Professor at Helwan University. His-research interests include micro/nano electronics, electronic design and analysis, VLSI technology, FPGA-based architectures, and embedded systems.